UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/536,627 | 05/08/2006 | Henri Vanderhenst | 016998-003900US | 9258 |

20350 7590 02/17/2009

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

| EXAMINER | |
|---|---|
| SHAH, TUSHAR S | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2184 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 02/17/2009 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/536,627 | VANDERHENST, HENRI | |
| | Examiner | Art Unit | |
| | TUSHAR S. SHAH | 2184 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

**DETAILED ACTION**

This action is in response to the amendment filed on November 28th, 2008.

***Status of Claims***

Claims 1-23 are presented for examination. Claims 1 and 23 are in independent form. Claims 1, 12, and 23 have been amended. Claims 1-23 are rejected under USC 103(a).

***Response to Arguments***

1. Applicant's arguments with respect to claim 1-23 have been considered but are moot in view of the new ground(s) of rejection.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1, 2, 9, 11, 13-15 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over European Publication No. EP 0 893 767 A2 (hereinafter Day) in view of Downie et al. UK Patent Application Publication No. GB 2 353 448 A (hereinafter Downie).

**Referring to claim 1**, Day discloses, A LIN bus system comprising a plurality of modules (plurality of circuit boards 12, Day column 2, lines 37-38) linked to a LIN bus along which electronic data or instructions can be sent to and from each said module,

at least one of said modules being non configured and having no unique identification address associated therewith (the circuit boards are assigned unique software address during start up, and therefore do no have a unique address prior to the power up procedure Day column 2, lines 48-51),

said at least one module having a unique code associated therewith (Each of the circuit boards 12 is loaded with a serial number which is stored in a non-volatile serial number register

14, Day column 2, lines 38-42), said system further including configuration means which interrogates said modules and detects the unique code of said at least one non-configured module and transmits a configuration signal to the module to configure the module (bus master device 20 issues an Assign Address command which utilizes the unique serial number which is stored on each circuit board, Day column 3, lines 43-45),

It is noted that Day does not appear to explicitly discloses, each said non-configured module including counter means which is incremented each time a non-configured module is configured, said counter of each non-configured module, once configured, providing a unique code which is indicative of the position of the module in the system.

However, Downie discloses, each said non-configured module including counter means which is incremented each time a non-configured module is configured, said counter of each non-configured module, once configured, providing a unique code which is indicative of the position of the module in the system (serial bus communications may use a counter to address nodes, wherein each node contains a counter, Downie column 2, lines 1-6) (The nodes in the system are addressed by an address command signal from the master and each module modifies the signal so it

is successively different from every preceding node, page 2, paragraph 2, lines 16-19).

Day and Downie are analogous art because they are from the same field of endeavor, namely a operating a bus with a single master and several slave nodes.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Downie and Day before him or her, to utilize the counter addressing means of Downie for the circuit boards in Day.

The suggestion/motivation for doing so is apparent, specifically in Downie Abstract paragraph 1, lines 1-3, that the method of Downie would minimize wiring and the complexity of the nodes.

Therefore it would have been obvious to combine Downie and Day to obtain the invention as disclosed in the instant claim.

**As per claim 2**, Day discloses, a LIN bus system as claimed in claim 1 wherein the at least one module having a unique code associated therewith is a reconfigurable module having means for being configured with an ID and also having embedded within it at the manufacturing stage a fixed unique Chip Identification Code (CIN) (Each of the circuit boards 12 is loaded with a serial number which is stored in a non-volatile serial number

register 14, Day column 2, lines 38-42) for use during a configuring operation (The serial number is used during power up of the system 10 to assign each circuit board 12 a unique software address which is stored in an address register 16, Day column 2, lines 48-52).

**As per claim 9**, it is noted that Day does not appear to explicitly disclose, said reconfigurable module further comprises a position counter, which may be incremented to indicate the position of the module in a daisy chain.

However, Downie discloses, a LIN bus system as claimed in claim 1 wherein said reconfigurable module further comprises a position counter, which may be incremented to indicate the position of the module in a daisy chain (serial bus communications may use a counter to address nodes, wherein each node contains a counter, Downie column 2, lines 1-6) (The nodes in the system are addressed by an address command signal from the master and each module modifies the signal so it is successively different from every preceding node, page 2, paragraph 2, lines 16-19).

Day and Downie are analogous art because they are from the same field of endeavor, namely a operating a bus with a single master and several slave nodes.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Downie and Day before him or her, to utilize the counter addressing means of Downie for the circuit boards in Day.

The suggestion/motivation for doing so is apparent, specifically in Downie Abstract paragraph 1, lines 1-3, that the method of Downie would minimize wiring and the complexity of the nodes.

Therefore it would have been obvious to combine Downie and Day to obtain the invention as disclosed in the instant claim.

**As per claim 11**, Day discloses, a LIN bus system as claimed in claim wherein said unique code is a CIN (Each of the circuit boards 12 is loaded with a serial number which is stored in a non-volatile serial number register 14, Day column 2, lines 38-42).

**As per claim 13**, it is noted that Day does not appear to explicitly disclose, a LIN bus system as claimed in claim 1, wherein said LIN Bus system comprises a plurality of non-configured reconfigurable modules connected together in a daisy chain manner.

However, Downie discloses, a LIN bus system as claimed in claim 1, wherein said LIN Bus system comprises a plurality of non-configured reconfigurable modules connected together in a daisy chain manner (The nodes are wired in a daisy chain fashion, Downie Abstract, paragraph 2, lines 1-2).

Day and Downie are analogous art because they are from the same field of endeavor, namely a operating a bus with a single master and several slave nodes.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Downie and Day before him or her, to utilize the counter addressing means of Downie for the circuit boards in Day.

The suggestion/motivation for doing so is apparent, specifically in Downie Abstract paragraph 1, lines 1-3, that the method of Downie would minimize wiring and the complexity of the nodes.

Therefore it would have been obvious to combine Downie and Day to obtain the invention as disclosed in the instant claim.

**As per claim 14**, Day discloses, a LIN bus system as claimed in claim 13 wherein a configuration sequence is performed to configure each of the plurality of non-configured reconfigurable modules (bus master device 20 issues an Assign Address command

which utilizes the unique serial number which is stored on each circuit board, Day column 3, lines 43-45).

**As per claim 15**, Day discloses, a LIN bus system as claimed in claim 14 wherein during a configuration sequence the bus master transmits a configuration request and all non-configured reconfigurable modules respond by transmitting a reply consisting of their unique code (the circuit boards 12 respond to the Assign Address command its unique serial number, Day column 3, lines 43-48).

**As per claim 19**, it is noted that Day does not appear to explicitly discloses, each non-configured reconfigurable module incorporates a position counter incremented on each occasion that a selected module responds with a forced current.

However, Downie discloses, a each non-configured reconfigurable module incorporates a position counter incremented on each occasion that a selected module responds with a forced current (serial bus communications may use a counter to address nodes, wherein each node contains a counter, Downie column 2, lines 1-6) (The nodes in the system are addressed by an address command signal from the master and each

module modifies the signal so it is successively different from every preceding node, page 2, paragraph 2, lines 16-19).

Day and Downie are analogous art because they are from the same field of endeavor, namely a operating a bus with a single master and several slave nodes.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Downie and Day before him or her, to utilize the counter addressing means of Downie for the circuit boards in Day.

The suggestion/motivation for doing so is apparent, specifically in Downie Abstract paragraph 1, lines 1-3, that the method of Downie would minimize wiring and the complexity of the nodes.

Therefore it would have been obvious to combine Downie and Day to obtain the invention as disclosed in the instant claim.

**As per claim 20**, Day discloses, a LIN bus system as claimed in claim 19 wherein the position counter on a particular non-configured reconfigurable module is not incremented when the particular non-configured reconfigurable module is itself selected (the unique software address is assigned once, at startup and does not need to change during the operation of the bus, Day column 3, lines 43-48).

**As per claim 21,** Day discloses, a LIN bus system as claimed in claim 20 wherein the position counter on a particular non-configured reconfigurable module is not incremented after the particular module has been selected (the unique software address is assigned once, at startup and does not need to change during the operation of the bus, Day column 3, lines 43-48).

**As per claim 22,** Day discloses, a LIN bus system as claimed in claim 21 wherein once all non-configured reconfigurable modules have been selected each will have a position counter showing a unique position for that module within a daisy chain and this unique position counter value is used to select a module and configure it for use in the system (Each circuit board on the bus is recognized by its unique software address, Day column 3, lines 10-12).

4. Claims 3-4, 6-8, 16-18 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Day in view of Downie, as applied to claim 1 above, further in view of De Haas et al. US Patent No. 6,664,821 B2 (hereinafter De Haas).

**As per claim 3,** Day and Downie do not appear to explicitly disclose, a LIN bus system as claimed in claim 2 wherein said

reconfigurable module is a module compatible with the LIN bus Standard.

However, De Haas discloses, a LIN bus system as claimed in claim 2 wherein said reconfigurable module is a module compatible with the LIN bus Standard (the line driver according to the invention is particularly useful in the LIN bus, De Haas column 2, lines 62-63).

Day, Downie and De Haas are analogous art because they are from the same field of endeavor, namely a operating a bus with a single master and several slave nodes.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Day and De Haas before him or her, to utilize the LIN protocol as apposed to $I^2C$.

The suggestion/motivation for doing so would have been that both $I^2C$ and Lin buses are well known for use in automotive applications.

Therefore it would have been obvious to combine Day, Downie and De Haas to arrive at the invention as specified in the instant claim.

**As per claim 4**, it is noted that Day does not appear to explicitly discloses, said

reconfigurable module has two LIN Bus interface pins connected by a series resistor.

However, Downie discloses, said reconfigurable module has two LIN Bus interface pins connected by a series resistor (Resistors 17, Downie Fig. 2).

Day and Downie are analogous art because they are from the same field of endeavor, namely a operating a bus with a single master and several slave nodes.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Downie and Day before him or her, to utilize the counter addressing means of Downie for the circuit boards in Day.

The suggestion/motivation for doing so is apparent, specifically in Downie Abstract paragraph 1, lines 1-3, that the method of Downie would minimize wiring and the complexity of the nodes.

Therefore it would have been obvious to combine Downie and Day to obtain the invention as disclosed in the instant claim.

**As per claim 6**, it is noted that Day and Downie do not appear to explicitly disclose, a LIN bus system as claimed in claim 1 wherein said reconfigurable module further comprises a

pull up resistor and a pull up current source for forcing a pull up current through the pull up resistor.

However, De Haas discloses, a LIN bus system as claimed in claim 1 wherein said reconfigurable module further comprises a pull up resistor (resistor R1, De Haas Fig. 2) and a pull up current source (T1, De Haas Fig. 2) for forcing a pull up current ($I_{LIN}$, De Haas Fig. 2) through the pull up resistor.

Day and De Haas are analogous art because they are from the same field of endeavor, namely a operating a bus with a single master and several slave nodes.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Day and De Haas before him or her, to utilize the LIN protocol as apposed to $I^2C$.

The suggestion/motivation for doing so would have been that both $I^2C$ and Lin buses are well known serial buses for use in automotive applications.

Therefore it would have been obvious to combine Day, Downie and De Haas to arrive at the invention as specified in the instant claim.

**As per claim 7**, Day discloses, a LIN bus system as claimed in claim 3, wherein if a number of said reconfigurable modules

are connected in a daisy chain manner standard LIN Bus arbitration rules apply for selecting one module from the daisy chain (the invention in Day discloses a bus master on a serial line with multiple slave nodes, this is seen as meeting the limitation, Day column 3, lines 10-17 and Fig. 1).

**As per claim 8**, it is noted that Day and Downie do not appear to explicitly disclose, a LIN bus system as claimed in claim 7 wherein said reconfigurable module further comprises a pull up resistor and a pull up current source for forcing a pull up current through the pull up resistor and wherein said pull up current only flows whilst said module is selected.

However, De Haas discloses, a LIN bus system as claimed in claim 7 wherein said reconfigurable module further comprises a pull up resistor (resistor R1, De Haas Fig. 2) and a pull up current source (T1, De Haas Fig. 2) for forcing a pull up current through the pull up resistor and wherein said pull up current only flows whilst said module is selected (Current $I_{LIN}$ is only greater than 0 when a signal is received on the TXD port sufficient to turn on transistor T1, De Haas Fig. 2).

Day and De Haas are analogous art because they are from the same field of endeavor, namely a operating a bus with a single master and several slave nodes.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Day and De Haas before him or her, to utilize the LIN protocol as apposed to $I^2C$.

The suggestion/motivation for doing so would have been that both $I^2C$ and Lin buses are well known serial buses for use in automotive applications.

Therefore it would have been obvious to combine Day, Downie and De Haas to arrive at the invention as specified in the instant claim.

**As per claim 16**, it is noted that Day and Downie do not appear to explicitly disclose, a LIN bus system as claimed in claim 15 wherein standard LIN bus arbitration rules apply, wherein active states win over recessive states, and one non-configured reconfigurable module will thus win the arbitration and become the selected module.

However, De Haas discloses, a LIN bus system as claimed in claim 15 wherein standard LIN bus arbitration rules apply, wherein active states win over recessive states, and one non-configured reconfigurable module will thus win the arbitration and become the selected module (This is seen as inherent to De Haas as it deals with a system conforming to the LIN Bus

specification and would therefore utilize these standard arbitration rules, De Haas column 2, lines 63-64).

Day, Downie and De Haas are analogous art because they are from the same field of endeavor, namely a operating a bus with a single master and several slave nodes.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Day and De Haas before him or her, to utilize the LIN protocol as apposed to $I^2C$.

The suggestion/motivation for doing so would have been that both $I^2C$ and Lin buses are well known serial buses for use in automotive applications.

Therefore it would have been obvious to combine Day, Downie and De Haas to arrive at the invention as specified in the instant claim.

**As per claim 17**, it is noted that Day and Downie do not appear to explicitly disclose, a LIN bus system as claimed in claim 16 wherein the selected module then forces a current through its pull up resistor.

However, De Haas discloses, a LIN bus system as claimed in claim 16 wherein the selected module then forces a current through its pull up resistor. (Current $I_{LIN}$ is only greater than

0 when a signal is received on the TXD port sufficient to turn on transistor T1, De Haas Fig. 2).

Day, Downie and De Haas are analogous art because they are from the same field of endeavor, namely a operating a bus with a single master and several slave nodes.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Day and De Haas before him or her, to utilize the LIN protocol as apposed to $I^2C$.

The suggestion/motivation for doing so would have been that both $I^2C$ and Lin buses are well known serial buses for use in automotive applications.

Therefore it would have been obvious to combine Day, Downie and De Haas to arrive at the invention as specified in the instant claim.

**As per claim 18,** Day does not appear to explicitly discloses, non-selected non-configured reconfigurable modules monitor the current through their series resistors and thereby determine that a selected module is responding.

However, Downie discloses, non-selected non-configured reconfigurable modules monitor the current through their series

resistors and thereby determine that a selected module is responding (Downie, Abstract paragraph 3, lines 1-5).

Day and Downie are analogous art because they are from the same field of endeavor, namely a operating a bus with a single master and several slave nodes.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Downie and Day before him or her, to utilize the counter addressing means of Downie for the circuit boards in Day.

The suggestion/motivation for doing so is apparent, specifically in Downie Abstract paragraph 1, lines 1-3, that the method of Downie would minimize wiring and the complexity of the nodes.

Therefore it would have been obvious to combine Downie and Day to obtain the invention as disclosed in the instant claim.

**Referring to claim 23,** Day discloses, a method of configuring a LIN Bus system
comprising a plurality of non-configured reconfigurable modules connected in a daisy chain manner comprising the steps of:

Transmitting a configuration request from a bus master (bus master device 20 issues an Assign Address command which utilizes

the unique serial number which is stored on each circuit board, Day column 3, lines 43-45);

It is noted that, Day does not appear to explicitly disclose, using the unique position counter value to select and configure a desired module or a plurality of desired modules

Incrementing a position counter of each module within the daisy chain that is not currently or previously selected;

Repeating the above steps until each module in the daisy chain has been selected, the position counters for each module thus showing its unique position in the chain.

However, Downie discloses, using the unique position counter value to select and configure a desired module or a plurality of desired modules (serial bus communications may use a counter to address nodes, wherein each node contains a counter, Downie column 2, lines 1-6)

Incrementing a position counter of each module within the daisy chain that is not currently or previously selected; and repeating the above steps until each module in the daisy chain has been selected, the position counters for each module thus showing its unique position in the chain (The nodes in the system are addressed by an address command signal from the master and each module modifies the signal so it is successively

different from every preceding node, page 2, paragraph 2, lines 16-19).

Day and Downie are analogous art because they are from the same field of endeavor, namely a operating a bus with a single master and several slave nodes.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Downie and Day before him or her, to utilize the counter addressing means of Downie for the circuit boards in Day.

The suggestion/motivation for doing so is apparent, specifically in Downie Abstract paragraph 1, lines 1-3, that the method of Downie would minimize wiring and the complexity of the nodes.

It is noted that Day and Downie do not appear to explicitly disclose, selecting one module from the daisy chain by standard LIN bus arbitration rules;

However, De Haas discloses, selecting one module from the daisy chain by standard LIN bus arbitration (This is seen as inherent to De Haas as it deals with a system conforming to the LIN Bus specification and would therefore utilize these standard arbitration rules, De Haas column 2, lines 63-64).

Day also does not appear to explicitly disclose, forcing a current through pull up resistor of the selected module;

However De Haas discloses, forcing a current through a pull up resistor of the selected module ($I_{LIN}$, De Haas Fig. 2).

Day, Downie and De Haas are analogous art because they are from the same field of endeavor, namely a operating a bus with a single master and several slave nodes.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Day and De Haas before him or her, to utilize the LIN protocol as apposed to $I^2C$.

The suggestion/motivation for doing so would have been that both $I^2C$ and Lin buses are well known serial buses for use in automotive applications.

Therefore it would have been obvious to combine Day, Downie and De Haas to arrive at the invention as specified in the instant claim.

5. Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Day in view of Downie as applied to claim 1 above, and further in view of Official Notice.

**As per claim 10**, neither Day nor Downie appears to explicitly disclose, a LIN bus system as claimed in claim 1 wherein said reconfigurable module further comprises a random code generator for generating a random code of a plurality of

bits in length to identify the module as an alternative to the CIN code.

However, it is seen as obvious that one of ordinary skill in the art the time of the invention would recognize that the unique software address generated in Day (Day column 2, lines 48-51), could be generated in any number of well know ways, including random number generation. The Examiner is taking official notice.

The suggestion/motivation for doing so would have been that using a random number generator to create an alternate ID for a node may allow for speedier and more efficient startup.

Therefore it would have been obvious to combine Day and De Haas to arrive at the invention as specified in the instant claim.

**As per claim 12**, similar limitations as in claim 10 are recited. Therefore the rejection of claim applies to claim 12.

6. Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Day in view of Downie, further in view of De Haas as applied to claim 4 above, and still further in view of Official Notice.

**As per claim 5**, neither Day nor De Haas appear to explicitly disclose, a LIN bus system as claimed in claim 4 wherein the series resistor is a 1 ohm resistor.

However, at the time of the invention, it would have been obvious to one of ordinary skill in the art to alter the value of the resistor R1 to be 1 ohm.

One of ordinary skill in the art would recognize that it would be obvious to try different resistance values during the design process in order to achieve the optimal result.

Therefore it would have been obvious to combine Day and De Haas to arrive at the invention as specified in the instant claim.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TUSHAR S. SHAH whose telephone number is (571)270-1970. The examiner can normally be reached on Mon-Fri 7:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on 571-272-4176. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T. S. S./
Examiner, Art Unit 2184

**/Henry W.H. Tsai/**
**Supervisory Patent Examiner, Art Unit 2184**